

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

Lead-Free

### DESCRIPTION

The TC55NEM216ATGN is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 1.8 μA standby current (typ) when chip enable ( $\overline{CE}$ ) is asserted high. There are two control inputs.  $\overline{CE}$  is used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control pin ( $\overline{LB}$ ,  $\overline{UB}$ ) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of -40° to 85°C, the TC55NEM216ATGN can be used in environments exhibiting extreme temperature conditions. The TC55NEM216ATGN is available in a plastic 54-pin thin-small-outline package (TSOP).

### FEATURES

- Low-power dissipation  
Operating: 15 mW/MHz (typical)
- Single power supply voltage of 5 V ± 10%
- Power down features using  $\overline{CE}$
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum): 20 μA

- Access Times (maximum):

	TC55NEM216ATGN	
	55	70
Access Time	55 ns	70 ns
$\overline{CE}$ Access Time	55 ns	70 ns
$\overline{OE}$ Access Time	30 ns	35 ns

- Package:  
TSOP II54-P-400-0.80 (Weight:0.57 g typ)
- Lead-Free

### PIN ASSIGNMENT (TOP VIEW)

#### 54 PIN TSOP

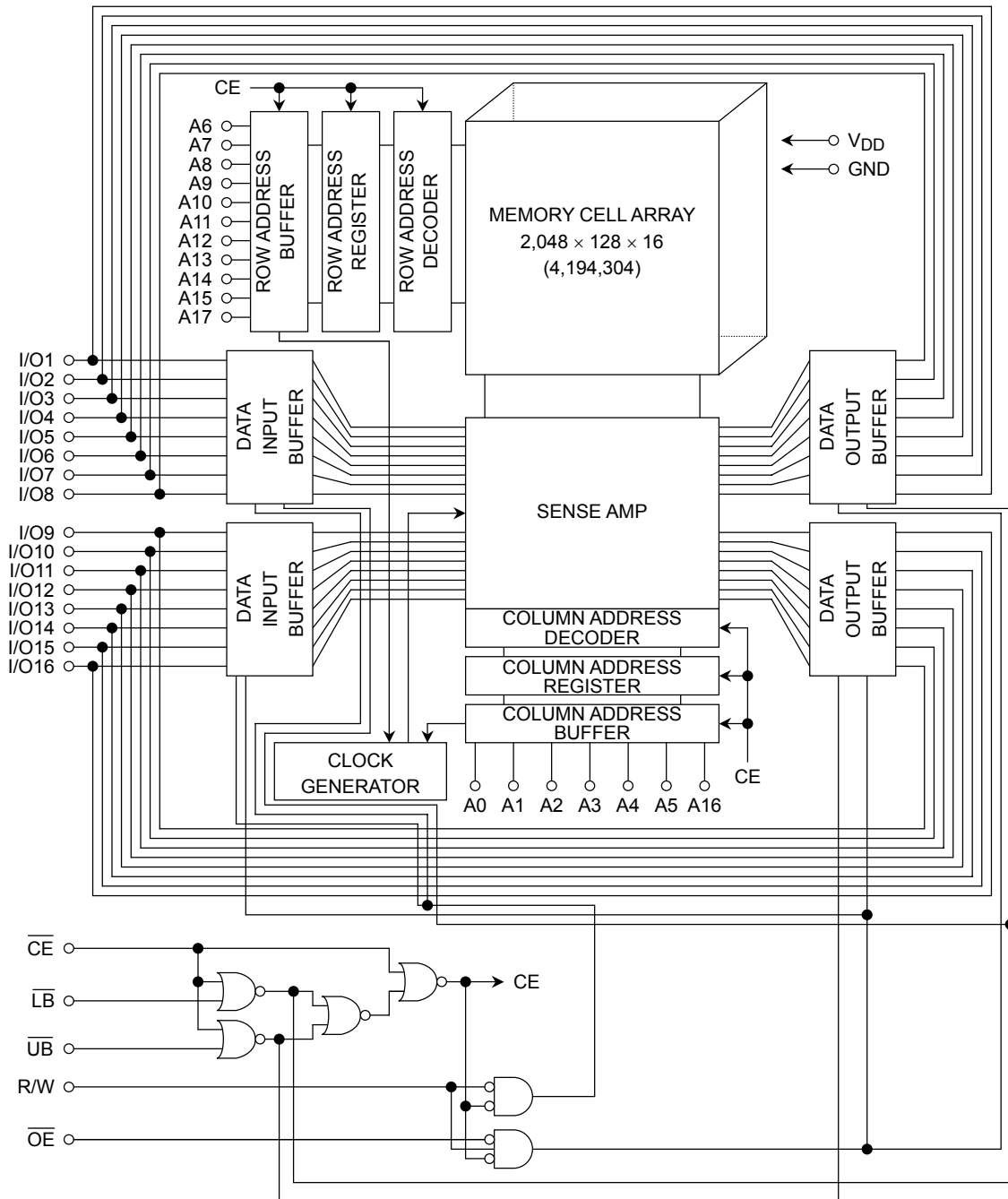
NC	1	○	54	□	A4
A3	2		53	□	A5
A2	3		52	□	A6
A1	4		51	□	A7
A0	5		50	□	NC
I/O16	6		49	□	I/O1
I/O15	7		48	□	I/O2
V <sub>DD</sub>	8		47	□	V <sub>DD</sub>
GND	9		46	□	GND
I/O14	10		45	□	I/O3
I/O13	11		44	□	I/O4
$\overline{UB}$	12		43	□	$\overline{LB}$
$\overline{CE}$	13		42	□	$\overline{OE}$
OP	14		41	□	OP
R/W	15		40	□	NC
I/O12	16		39	□	I/O5
I/O11	17		38	□	I/O6
GND	18		37	□	GND
V <sub>DD</sub>	19		36	□	V <sub>DD</sub>
I/O10	20		35	□	I/O7
I/O9	21		34	□	I/O8
NC	22		33	□	A8
A17	23		32	□	A9
A16	24		31	□	A10
A15	25		30	□	A11
A14	26		29	□	A12
A13	27		28	□	NC

### PIN NAMES

A0~A17	Address Inputs
$\overline{CE}$	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$ , $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V <sub>DD</sub>	Power (+5 V)
GND	Ground
NC	No Connection
OP*	Option

\*: OP pin must be open or connected to GND.

**BLOCK DIAGRAM**



## OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	L	H	L	L	Output	Output	I <sub>DDO</sub>
	L	L	H	H	L	High-Z	Output	I <sub>DDO</sub>
	L	L	H	L	H	Output	High-Z	I <sub>DDO</sub>
Write	L	*	L	L	L	Input	Input	I <sub>DDO</sub>
	L	*	L	H	L	High-Z	Input	I <sub>DDO</sub>
	L	*	L	L	H	Input	High-Z	I <sub>DDO</sub>
Output Deselect	L	H	H	L	L	High-Z	High-Z	I <sub>DDO</sub>
	L	H	H	H	L	High-Z	High-Z	I <sub>DDO</sub>
	L	H	H	L	H	High-Z	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	*	High-Z	High-Z	I <sub>DDS</sub>
	*	*	*	H	H	High-Z	High-Z	I <sub>DDS</sub>

\* = don't care  
H = logic high  
L = logic low

## MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-0.3*~7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.5~V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10s)	260	°C
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	-40~85	°C

\*: -2.0 V when measured at a pulse width of 20ns

## DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.4	—	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	0.6	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

\*: -2.0 V when measured at a pulse width of 20ns

## DC CHARACTERISTICS (Ta = -40° to 85°C, VDD = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V		-1.0	—	—	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V		2.1	—	—	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{LB} = \overline{UB} = V_{IH}$ or $R/W = V_{IL}$ or $OE = V_{IH}$ , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ and $R/W = V_{IH}$ , $\overline{LB} = \overline{UB} = V_{IL}$ , I <sub>OUT</sub> = 0 mA, Other Input = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub>	MIN	—	—	35	mA
				1 μs	—	8	—	
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2$ V and $R/W = V_{DD} - 0.2$ V, $\overline{LB} = \overline{UB} = 0.2$ V, I <sub>OUT</sub> = 0 mA, Other Input = V <sub>DD</sub> - 0.2 V/0.2 V	t <sub>cycle</sub>	MIN	—	—	30	mA
				1 μs	—	3	—	
I <sub>DDS1</sub>	Standby Current	1) $\overline{CE} = V_{IH}$ 2) $\overline{LB} = \overline{UB} = V_{IH}$		—	—	3	mA	
I <sub>DDS2</sub>		1) $\overline{CE} = V_{DD} - 0.2$ V		Ta = 25°C	—	1.8	—	μA
		2) $\overline{LB} = \overline{UB} = V_{DD} - 0.2$ V, $\overline{CE} = 0.2$ V		Ta = -40~40°C	—	—	3	
			Ta = -40~85°C	—	—	20		

## CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

## AC CHARACTERISTICS AND OPERATING CONDITIONS

( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ )

### READ CYCLE

SYMBOL	PARAMETER	TC55NEM216ATGN				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	55	—	70	—	ns
$t_{ACC}$	Address Access Time	—	55	—	70	
$t_{CO}$	Chip Enable Access Time	—	55	—	70	
$t_{OE}$	Output Enable Access Time	—	30	—	35	
$t_{BA}$	Data Byte Control Access Time	—	55	—	70	
$t_{COE}$	Chip Enable Low to Output Active	5	—	5	—	
$t_{OEE}$	Output Enable Low to Output Active	0	—	0	—	
$t_{BE}$	Data Byte Control Low to Output Active	5	—	5	—	
$t_{OD}$	Chip Enable High to Output High-Z	—	25	—	30	
$t_{ODO}$	Output Enable High to Output High-Z	—	25	—	30	
$t_{BD}$	Data Byte Control High to Output High-Z	—	25	—	30	
$t_{OH}$	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC55NEM216ATGN				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time	55	—	70	—	ns
$t_{WP}$	Write Pulse Width	40	—	50	—	
$t_{CW}$	Chip Enable to End of Write	45	—	55	—	
$t_{BW}$	Data Byte Control to End of Write	45	—	55	—	
$t_{AS}$	Address Setup Time	0	—	0	—	
$t_{WR}$	Write Recovery Time	0	—	0	—	
$t_{ODW}$	R/W Low to Output High-Z	—	25	—	30	
$t_{OEW}$	R/W High to Output Active	0	—	0	—	
$t_{DS}$	Data Setup Time	25	—	30	—	
$t_{DH}$	Data Hold Time	0	—	0	—	

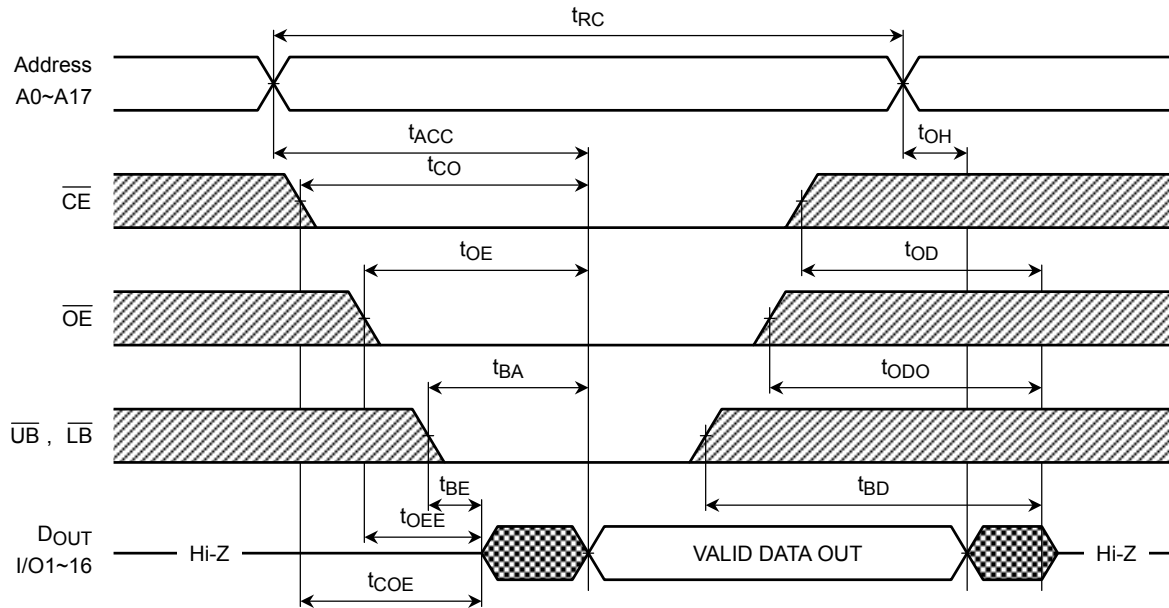
Note:  $t_{OD}$ ,  $t_{ODO}$ ,  $t_{BD}$  and  $t_{ODW}$  are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

### AC TEST CONDITIONS

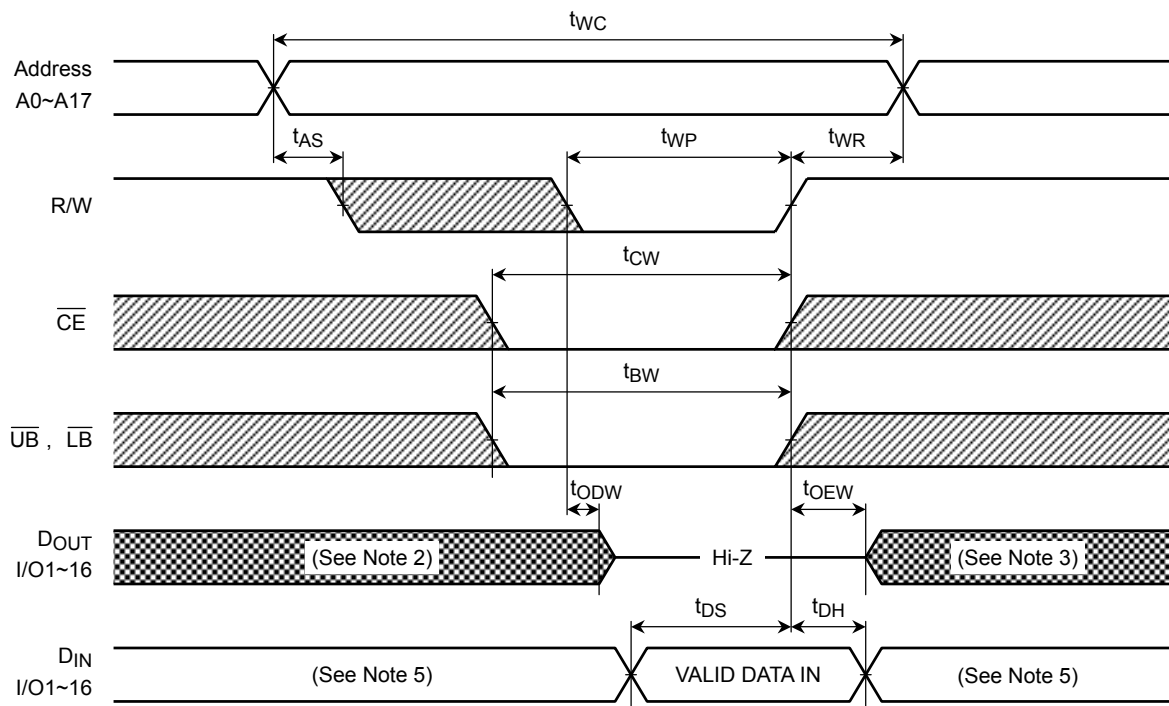
PARAMETER	TEST CONDITION
Input pulse level	0.4 V, 2.6 V
$t_R$ , $t_F$	5 ns
Timing measurements	1.5 V
Reference level	1.5 V
Output load	30 pF + 1 TTL Gate (55) 100 pF + 1 TTL Gate (70)

## TIMING DIAGRAMS

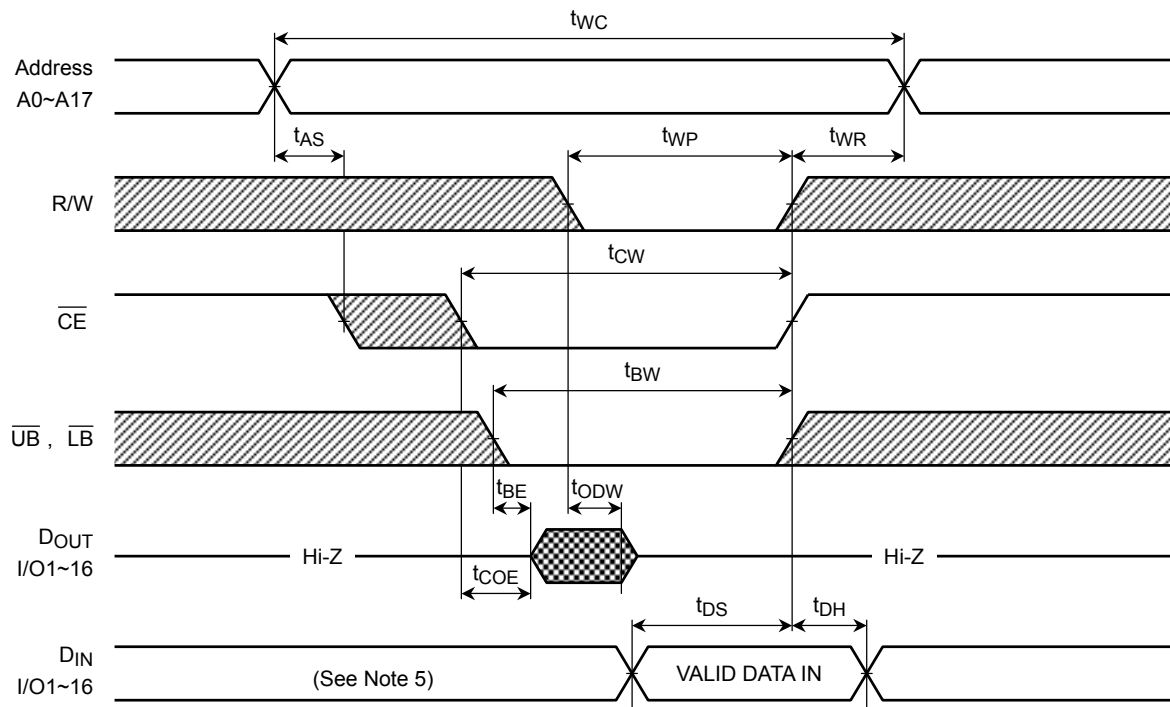
### READ CYCLE (See Note 1)



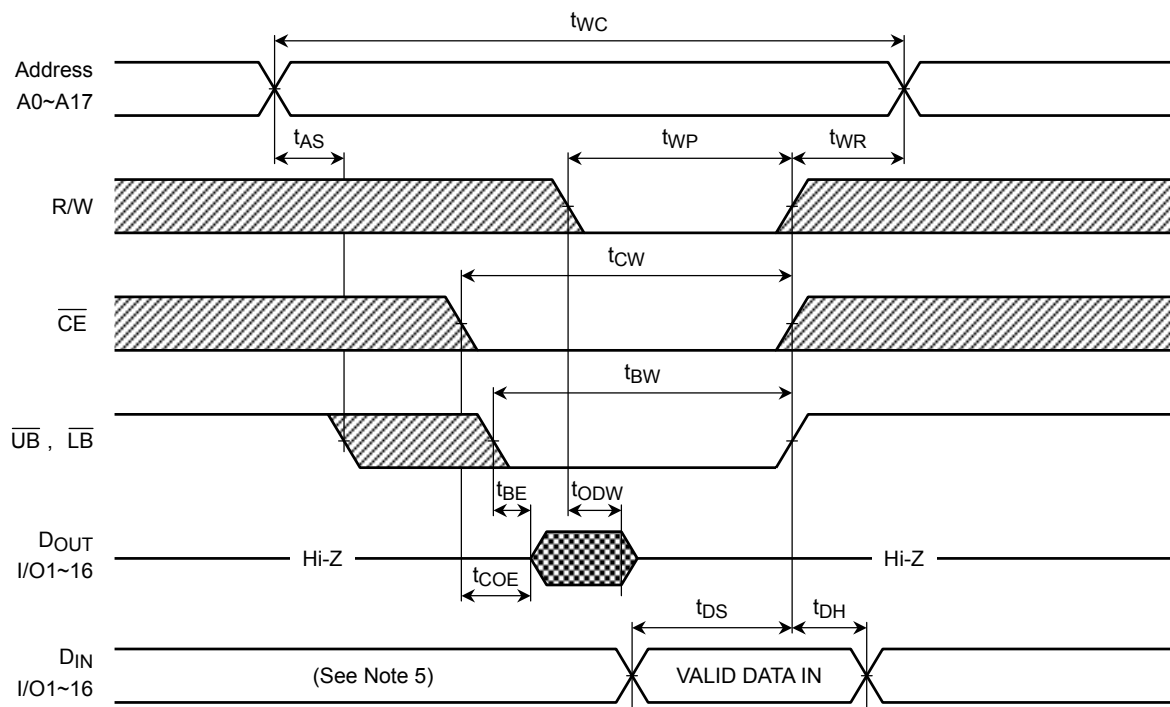
### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



## WRITE CYCLE 2 ( $\overline{CE}$ CONTROLLED) (See Note 4)



## WRITE CYCLE 3 ( $\overline{UB}$ , $\overline{LB}$ CONTROLLED) (See Note 4)



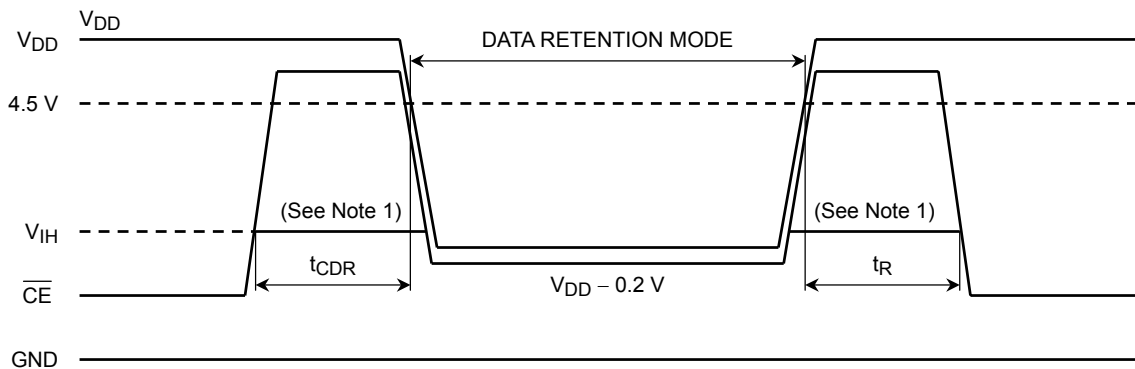
Note:

- (1) R/W remains HIGH for the read cycle.
- (2) If  $\overline{CE}$  (or  $\overline{UB}$  or  $\overline{LB}$ ) goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If  $\overline{CE}$  (or  $\overline{UB}$  or  $\overline{LB}$ ) goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

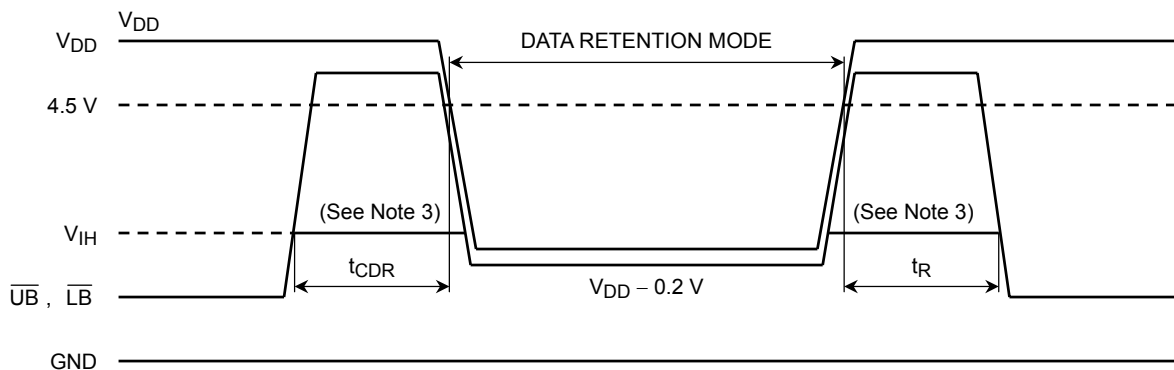
## DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V
I <sub>DD</sub> S2	Standby Current	Ta = -40~40°C	—	3	μA
		Ta = -40~85°C	—	20	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time	0	—	—	ns
t <sub>R</sub>	Recovery Time	5	—	—	ms

### $\overline{CE}$ CONTROLLED DATA RETENTION MODE



### $\overline{UB}, \overline{LB}$ CONTROLLED DATA RETENTION MODE (See Note 2)





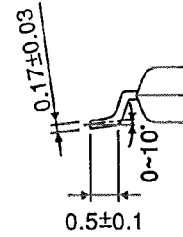
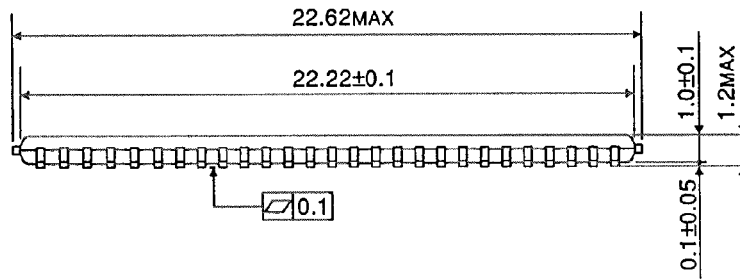
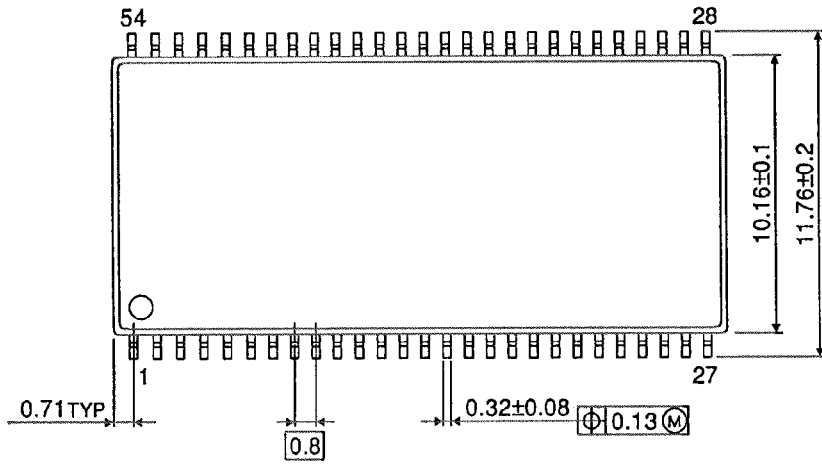
## Note:

- (1) When  $\overline{CE}$  is operating at the  $V_{IH}(\text{min.})$  level(2.4 V), the operating current is given by  $I_{DDs1}$  during the transition of  $V_{DD}$  from 4.5 to 2.6 V.
- (2) In  $\overline{UB}$  (or  $\overline{LB}$ ) controlled data retention mode, minimum standby current mode is entered when  $\overline{CE} \leq 0.2 \text{ V}$  or  $\overline{CE} \geq V_{DD} - 0.2 \text{ V}$ .
- (3) When  $\overline{UB}$  (or  $\overline{LB}$ ) is operating at the  $V_{IH}(\text{min.})$  level(2.4 V), the operating current is given by  $I_{DDs1}$  during the transition of  $V_{DD}$  from 4.5 to 2.6 V.

## PACKAGE DIMENSIONS

TSOPII54-P-400-0.80

Unit: mm



Weight:0.57 g (typ)

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